Abstract of the Disclosure:

A self-test circuit has an address generator unit for generating a test address for the purpose of testing a memory circuit and a control circuit that has signal inputs via which test commands can be applied and via which a memory access may be carried out. A first register is provided for storing an address difference value, in which case, as a result of a first test command, the address generator circuit increases the test address by the address difference value in the event of a subsequent memory access or, as a result of a second test command, the address generator circuit decreases the test address by the address difference value in the event of a subsequent memory access.

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